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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,732	09/30/2003	David Arnold Luick	ROC920030254US1	6370

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EXAMINER	
GU, SHAWN X	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 04/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No.	Applicant(s)	
	10/675,732	LUICK, DAVID ARNOLD	
	Examiner	Art Unit	
	Shawn Gu	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31,33 and 34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-10,17-23,33 and 34* is/are allowed.

6)☒ Claim(s) *11,16,24,25 and 29-31* is/are rejected.

7)☒ Claim(s) *12-15 and 26-28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This final Office action is in response to the amendment filed 24 March 2006. Claims 1-31, 33 and 34 are pending. All objections and rejections not repeated below are withdrawn.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1, 5, 6, 7, 14 and 15 of U.S. Patent Application 10675170 (hereinafter "'170") contain every element of claims 11 and 16 of the instant application and as such provisionally anticipate claims 11 and 16 of the instant application.

"A later patent claim is not patentably distinct from an earlier patent claim if the later claim is obvious over, or **anticipated by**, the earlier claim. In re Longi, 759 F.2d at 896, 225 USPQ at 651 (affirming a holding of obviousness-type double patenting because the claims at issue were obvious over claims in four prior art patents); In re Berg, 140 F.3d at 1437, 46 USPQ2d at 1233 (Fed. Cir. 1998) (affirming a holding of obviousness-type double patenting where a patent application claim to a genus is anticipated by a patent claim to a species within that genus). " ELI LILLY AND COMPANY v BARR LABORATORIES, INC., United States Court of Appeals for the Federal Circuit, ON PETITION FOR REHEARING EN BANC (DECIDED: May 30, 2001).

Claim 11 of the instant application is anticipated by claims 1, 5 and 6, and 14 of '170. The case for an obviousness-type double patent is made clear when claim 6 of '170 defined the "pre-fetch data" of claims 1 and 5 as "a plurality of up-or-down counters corresponding to respective sub-units of the segment". A sub-unit of claim 1 of '170 is defined as "an integral number of pages", and the claim further discloses pre-fetching data with respect to a sub-unit (page) using said pre-fetch data, therefore the combination of claims 1, 5 and 6 of '170 clearly anticipates claim 11 of the instant claim.

Claim 16 of the instant application is anticipated by claims 1, 5, 6 and 7, and 15 of '170. Claim 7 of '170, which is dependent on claims 1, 5 and 6, and claim 15 of '170 both anticipate every limitation of claim 16 of the instant application.

Although claims 11 and 16 of the instant application both claim a method, it is clear that in '170, the digital data processing device of claims 1, 5, 6 and 7, and the processor of claims 14 and 15 perform the said method.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 24, 25, 29 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Doing et al. [6,161,166] (hereinafter "Doing"), in further view of Kedem et al. [6,134,643] (hereinafter "Kedem") and Schumann et al. [6,012,106] (hereinafter "Schumann").

As for claim 24, Doing teaches a digital data processing device, comprising:

at least one processor which generates memory references to memory address locations (Fig 1A and Fig 2, 101 CPU);

a memory (Fig 1A and Fig 1B, 102 Main Memory), said memory containing a page table, said page table having a plurality of page table entries corresponding to addressable pages (Fig 8, 822 Page Table); and

at least one cache for temporarily storing data from said memory for use in satisfying memory references generated by said at least one processor (Fig 1A, 108 L2 cache). Doing does not teach a pre-fetch engine or persistent reference history data contained in each page table entry.

However, Kedem teaches a digital data processing device which comprises a pre-fetch engine (Fig 1, combination of 30 Prefetch Controller, 40 Prediction Table, and 35 Prefetch Buffer), said pre-fetch engine pre-fetching data from addressable pages to at least one cache using persistent reference history data with respect to the corresponding addressable page, said persistent reference history data being maintained throughout the life of the corresponding addressable page in memory (Col 3, Lines 22-42), in order to improve access latency without significantly affecting the operation of the processor (Col 3, Lines 10-21). Therefore, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to incorporate Kedem's pre-fetch engine and persistent reference history data with Doing's digital data processing device to improve access latency. Yet, Kedem does not teach that the

persistent history data used by the pre-fetch engine is contained in each of at least some of said page table entries.

However, Schumann teaches a digital data processing device which comprises pre-fetching data from addressable pages using persistent reference history data with respect to the corresponding addressable page, the persistent reference history data contained at least some of said page table entries in a page table, the persistent reference history data being maintained throughout the life of the corresponding addressable page in memory (Fig 2, Prefetch Length in 21 Page Table; Prefetch Length records the number of actual cache lines accessed, which indicate memory references by the processor; see Abstract; and Col 4, Lines 18-63), with the intention to reduce the number of wait states and improve access time (see Abstract), and to further improve cache throughput (Col 1, Lines 60-65). Furthermore, keeping the persistent reference history data in cache as disclosed in Kedem increases design complexity since that would further require deciding the size of the prediction table and replacement algorithm (Kedem, Col 3, Lines 43-49). Therefore, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to combine Doing's teaching in combination with the teachings of Kedem and Schumann for the above mentioned reasons, which include reducing number of wait states, improving access time and cache throughput, and further reducing design complexity. Hence to summarize, by including Kedem's Pre-fetch engine and Schumann's persistent reference history data with Doing's digital processing device, the combined references teach a memory page table having a plurality of page table entries corresponding to addressable pages,

wherein each of at least some of said page table entries contains persistent reference history data with respect to memory references generated by said at least one processor to memory address locations within the corresponding addressable page, said persistent reference history data being maintained throughout the life of the corresponding addressable page in memory.

As for claim 25, Doing further teaches the said digital data processing system comprises a plurality of processors (Fig 1B, 101A-101D CPUs; Col 6, Lines 15-19), and it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention that the said persistent history data is based on reference events occurring in said plurality of processors, since the plurality of processors all make references to the same memory (Fig 1B, 102 Main Memory).

As for claim 29, Doing further teaches the said digital data processing device comprises a plurality of caches at a plurality of cache levels (Fig 1A, 106 L1 I-cache, 107 L1 D-cache, and 108 L2 cache), and it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention that said pre-fetch engine taught in claim 24 pre-fetches data to different cache levels, as both L1 and L2 caches access the same memory (Fig 1B, 102 Main Memory) which contains the page table that holds persistent reference history data for pre-fetching to cache.

As for claim 30, Doing further teaches the digital data processing system further comprises:

an address translation mechanism which translates effective addresses in an address space of a task executing on said at least one processor to virtual addresses in a global address space of said digital processing system, and translates said virtual addresses to real addresses corresponding to physical memory locations in said memory (Figs 4-8).

6. Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Doing in combination with Kedem and Schumann, in further view of "Computer Architecture A Quantitative Approach" [by David A. Patterson and John L. Hennessy] (hereinafter "Patterson") and Chauvel [US 6,957,315 B2] (hereinafter "Chauvel").

As for claim 31, Doing in combination of Kedem and Schumann already substantially disclosed the claim as described above, but do not particularly point out that the said pre-fetch engine pre-fetches address translation data into at least one address translation cache structure of said address translation mechanism. However, Patterson discloses that in a virtual memory system such as that of Doing's, a TLB (Translation Look-aside Buffer) that contains address translation data is included to improve address translation latency (Pages 445-446). Chauvel further teaches pre-fetching TLB entries to prevent TLB misses (Col 8, Lines 18-22).

Therefore it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention that Patterson and Chauvel's teachings can be combined with those of Doing, Kedem, and Schumann, in order to improve address translation latency and prevent TLB misses.

Allowable Subject Matter

7. Claims 1-10, 17-23, 33 and 34 are allowed.

8. Claims 12-15 and 26-28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is an examiner's statement of reasons for allowance:

As for claims 1, 17 and 33, the combined references of Doing et al. [6,161,166], Kedem et al. [6,134,643] and Schumann et al. [6,012,106] teach most of the limitations of the claims as described by the first Office Action's rejection over the original claims 24 and 32, however the reference history data disclosed by the combined references are not contained in the page table entries, respectively for each of a plurality of cacheable sub-units of the corresponding addressable pages. Instead the reference history data in the combined references is for the entire page as a whole (see Kedem et

al., column 3, lines 22-42; and Schumann et al., fig 2, Prefetch Length in 21 Page Table, and column 4, lines 18-63).

As for claim 34, the combined references Doing et al., Kedem et al., and Schumann et al. teach every limitation of the claim except that the counter of the combined references is only an up-counter instead of an up-or-down counter (see Kedem, Fig 2, Item 55), and there is no second type of event to trigger the decrement of the counter.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

10. Applicant's arguments regarding claim 24 have been considered, but the newly added limitations are taught by Doing et al., in further view of Kedem et al., and Schumann et al. as set forth above.

Furthermore, claims 11-16 are no longer allowable due to the double patenting rejections raised in response to amendments made to the pending U.S. Patent Application 10675170.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shawn Gu whose telephone number is (571) 272-0703. The examiner can normally be reached on 9am-5pm, Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon can be reached on (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shawn X Gu
Patent Examiner
Art Unit 2189

Reginald G. Bragdon
REGINALD G. BRAGDON
PRIMARY EXAMINER

5 April 2006